IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	GEISSINGER, JOHN D.		
Application No.:	09/491302	Group Art Unit:	2815
Filed:	January 25, 2000	Examiner:	Paul E. Brock II
Title:	ELECTRONIC PACKAGE WITH INTEGRATED CAPACITOR		

BRIEF ON APPEAL

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8-18-05 — Melanie Gover

Date — Signed by: Melanie G. Gover

Dear Sir:

This is an appeal from the Office Action mailed on March 8, 2005, finally rejecting claims 1-4 and 8-19.

A Notice of Appeal in this application was mailed on June 3, 2005, and was received in the USPTO on June 3, 2005.

The fee required under 37 CFR § 41.20(b)(2) for filing an appeal brief should be charged to Deposit Account No. 13-3723. Any extension fees or other fees due should also be charged to Deposit Account No. 13-3723.

Appellants request the opportunity for a personal appearance before the Board of Appeals to argue the issues of this appeal. The fee for the personal appearance will be timely paid upon receipt of the Examiner's Answer.

REAL PARTY IN INTEREST

The real party in interest is 3M Company (formerly known as Minnesota Mining and Manufacturing Company) of St. Paul, Minnesota and its affiliate 3M Innovative Properties Company of St. Paul, Minnesota.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1 to 4 and 8 to 19 are pending.

SUMMARY OF CLAIMED SUBJECT MATTER

The claims at issue concern electronic packages and more specifically an electronic package with an integrated capacitor.

Claim 1 provides an electronic package, comprising: a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads; a dielectric substrate mounted on the first side of the conductive trace layer; an embedded capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm., including a first conductive layer, a second conductive layer and a layer of dielectric material made of a non-conductive polymer blended with high dielectric constant particles disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer; a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions. This invention is described in the specification, for example, at page 3, line 20 to p. 4, line 7 and p. 7, lines 6-9.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Sole Ground of Rejection

Claims 1 to 4 and 8 to 19 stand rejected under 35 USC § 103(a) as purportedly unpatentable over the combined teachings of Schueller et al. (USPAT 5844168, Schueller) in view of Brandt et al. (USPAT 6068782, Brandt).

ARGUMENT

Background

Electronic packages facilitate the mounting and handling of electronic devices such as microprocessors, video controllers and memory. Capacitors are used to decouple the system-level power supply from individual electrical devices of an electronic package. Decoupling of an electronic device from the power supply reduces the overall noise in the power distribution network of the electronic package. However, due to increases in the speed and electrical current associated with high-speed electronic devices, traditional capacitor structures do not provide adequate performance because the inductance associated with these types of capacitors inhibits their operation at high speeds. Interconnect inductance in an electronic package chokes the capacitor, preventing the high-speed transfer of electrical current to and from the capacitor.

Embedding capacitors directly into the electronic packages provides significant decoupling capacitance with very low interconnect inductance. Furthermore, the electrodes of the capacitor may serve as reference voltage planes in the electronic package for providing excellent power distribution within the package. This approach facilitates very high-speed operation of electronic devices within an electronic package.

Sole Ground of Rejection

Claims 1 to 4 and 8 to 19 stand rejected under 35 USC 103(a), as purportedly unpatentable over the combined teachings of Schueller et al. (USPAT 5844168, Schueller) in view of Brandt et al. (USPAT 6068782, Brandt).

Applicants assert that the rejection of claims 1 to 4 and 8 to 19 under 35 USC § 103 (a) should be reversed for the following reasons.

The Office Action states in part:

> With regard to claim 1, Schueller discloses in figures 7 -7b an electronic package. Schueller discloses in figures 7 -7b a conductive trace layer (720b) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads. Schueller discloses in figures 7 -7b a dielectric substrate (720a) mounted on the first side of the conductive trace layer. Schueller discloses in figures 7 -7b and column 8, lines 42 -44 an embedded capacitor (bottom layer of 710, top layer of 700, and the bottom layer of 700) having a capacitance including a first conductive layer (bottom layer of 710), a second conductive layer (bottom layer of 700) and a layer of dielectric material (top layer of 700) made of a non-conductive polymer (polyimide, top layer of 700) disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer (725). It is inherent in the method of Schueller that the bottom layer of 710, top layer of 700, and the bottom layer of 700 form a capacitor because this configuration is the definition of a capacitor. Schueller is silent to teaching a specific capacitance and a dielectric material made of a non-conductive polymer blended with high dielectric constant particles. Brandt teaches in column 4, lines 18-41 and column a suitable dielectric material made of a non-conductive polymer blended with high dielectric particles. Brandt further teaches in column 6, lines 44-60 a capacitor with this dielectric layer having a capacitance of 200 nF/sq.cm (500 pF is equivalent to 50 nF, (50 nF)/(0.25 cm^2) = 200 nF/cm^2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material and capacitance of Brandt in the method of Kling (sic) in order to tune the electronic properties of a capacitor component as stated by Brandt in column 4, lines 22 -41. It further would have been obvious to one of ordinary skill in the art at the time of the present invention to use a capacitance of from about 1nF/sq.cm to about 100 nF/sq.cm in order to optimize the capacitance, and because Brandt teaches optimization in column 4, lines 37 –41 (also see MPEP 2144.05). Schueller discloses in figures 7 -7b a plurality of interconnect regions (741 and 742) extending through the first conductive layer and the dielectric material layer of the capacitor. Schueller discloses in figures 7 -7b an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected (750) to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected (751) to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

Applicants submit that according to MPEP 2142, to establish a case of prima facie obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co., 226 USPQ 438 (PTO Bd. App. 1984).*

Applicants respectfully submit that the references cannot support a case of *prima facie* obviousness as to the claims because, among other possible reasons, the cited references do not

provide a motivation or suggest for embedding a capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. in the structure of Schueller. Although two metal layers separated by an insulating layer may have nominal capacitance, contrary to the Examiner's statements, nowhere does Schueller indicate that it is using, or seeks to use, its metal and dielectric layers as a capacitor. Instead, Schueller teaches a BGA package in which a stiffener layer is also used as a conductive layer. In some embodiments, TAB tapes are used to form additional conductive layers. Accordingly, there would be no motivation based on the teachings of Schueller to "use the dielectric material and capacitance of Brandt in the method of Kling (sic) in order to tune the electronic properties of a capacitor component as stated by Brandt in column 4, lines 22 -41" with respect to the layers in the Schueller article to make them into a capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. Applicants respectfull submit that the Examiner is taking the teachings of Schueller out of context to argue that the metal layer and dielectric layer of one TAB tape, plus the metal layer of an adjacent TAB tape form a capacitor.

CONCLUSION

For the foregoing reasons, appellants respectfully submit that the Examiner has erred in rejecting this application. Please reverse the Examiner on all counts.

Respectfully submitted,

August 18, 2005
Date

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CLAIMS APPENDIX

1. (Previously presented) An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a dielectric substrate mounted on the first side of the conductive trace layer;

an embedded capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm., including a first conductive layer, a second conductive layer and a layer of dielectric material made of a non-conductive polymer blended with high dielectric constant particles disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

2. (Original) The electronic package of claim 1 wherein the first electrode is maintained at a first reference voltage and wherein the second electrode is maintained at a second reference voltage different from the first reference voltage.

3. (Previously presented) The electronic package of claim 1 further comprising an electrically conductive stiffening member attached to the second conductive layer of the capacitor by a second adhesive layer.

4. (Previously presented) The electronic package of claim 3 further comprising a device receiving region extending through the dielectric substrate, the conductive trace layer and the

capacitor, and further comprising an electronic device attached to the device receiving region on the stiffening member by a third adhesive layer.

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Original) The electronic package of claim 1 wherein the capacitor has a capacitance of from about 2 nF/sq. cm. to about 30 nF/sq. cm.

9. (Original) The electronic package of claim 1 wherein the capacitor has a capacitance of from about 5 nF/sq. cm. to about 15 nF/sq. cm.

10. (Original) The electronic package of claim 1 wherein the capacitor has a capacitance of at least 30nF/sq. cm.

11. (Previously presented) The electronic package of claim 1 wherein the dielectric material of the capacitor has a thickness of from about 0.5 um to about 30 um.

12. (Original) The electronic package of claim 1 wherein the dielectric material of the capacitor includes a metal oxide.

13. (Previously presented) The electronic package of claim 1 wherein the dielectric constant particles are formed from a material selected from the group consisting of barium titanate, barium strontium titanate, titanium oxide, lead zirconium titanate and tantalum oxide.

14. (Original) The electronic package of claim 1 wherein the dielectric substrate includes a plurality of apertures, each one of the apertures being positioned adjacent to one of the interconnect region of the capacitor.

15. (Original) The electronic package of claim 1 wherein the dielectric substrate includes a polymeric film.

16. (Original) The electronic package of claim 15 wherein said polymeric film is polyimide film.

17. (Original) The electronic package of claim 1 wherein the interconnect member is a solder plug.

18. (Original) The electronic package of claim 1 wherein each interconnect pad is a solderball pad.

19. (Previously presented) The electronic package of claim 18 wherein the dielectric substrate has an aperture extending therethrough adjacent to each solderball pad.

20. (Cancelled)

21. (Cancelled).

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)